forming an interlayer film on said substrate at said CMOS logic circuit portion and on said substrate at said DRAM portion, covering said first transistor and said second transistor;

forming a groove in said interlayer film by removing a portion of said interlayer film at said DRAM portion;

forming a first polysilicon film on an upper surface of said interlayer film at said CMOS logic circuit portion and at said DRAM portion, and a second polysilicon film on an inner wall of said groove at said DRAM portion,

forming a first HSG on a surface of said first polysilicon film and a second HSG on a surface of said second polysilicon film;

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removing said first HSG and said first polysilicon film

forming a capacitor dielectric film n said HSG after removing said first HSG and said first polysilicon film; and

forming an upper electrode on said capacitor dielectric film.

2.(Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 1,

wherein said step of forming said first transistor includes a step of forming a first gate insulating layer, and

wherein said step of forming said second transistor includes a step of forming a second gate insulating layer,

wherein said first gate insulating layer is thinner that said second gate insulating layer.

3. (Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 2,

wherein said second transistor comprises a peripheral circuit transistor and a switching transistor, and

wherein said peripheral circuit transistor and said switching transistor have similar structures.

7. (Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 6, further comprising steps of:

forming a first photoresist layer on said first HSG and a second photoresist layer on said second HSG; and

removing said first photoresist layer to expose said first HSG.

9. (Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 7, wherein said capacitor dielectric film comprises a Ta2O5 film.

16. (Amended) A method of manufacturing a system-on-chip semiconductor device including a CMOS logic circuit and a DRAM on the same semiconductor chip, said DRAM comprising a cylinder type capacitor, the method comprising the steps of:

providing a CMOS logic circuit portion and a DRAM portion on a substrate;

forming a first transistor on a substrate at said CMOS logic circuit portion;

forming a second transistor on said substrate at said DRAM portion;

forming an interlayer film on said substrate at said CMOS logic circuit portion and on said substrate at said DRAM portion, covering said first transistor and said second transistor;

forming a groove in said interlayer film by removing a portion of said interlayer film at said DRAM portion;

forming a polysilicon film on said interlayer film at said CMOS logic circuit portion and at said DRAM portion, and on an inner wall of said groove at said DRAM portion,

forming an HSG on a surface of said polysilicon film;

removing said HSG and said polysilicon film from an upper surface of said interlayer film, retaining at least a portion of said HSG in said groove and at least a portion said polysilicon in said groove; and

forming a capacitor dielectric film on said portion of said HSG in said groove after removing said HSG and said polysilicon film.

17. (Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 16,

wherein said step of forming said first transistor includes a step of forming a first gate insulating layer, and

wherein said step of forming said second transistor includes a step of forming a second gate insulating layer,

wherein said first gate insulating layer is thinner that said second gate insulating layer.

Please add the following new claims:

20. (New) The method as claimed in claim 2, wherein said first transistor comprises a p-type transistor having a gate electrode which is made of polysilicon doped with boron, and an n-type transistor having a gate electrode which is made of polysilicon doped with phosphorous.

21. (New) The method as claims in claim 20, wherein said second transistor comprises a p-type transistor having a gate electrode which is made of polysilicon doped with phosphorous.